64 % EFFICIENCY ENHANCEMENT-MODE POWER HETEROJUNCTION FET FOR 3.5 V Li-ION BATTERY OPERATED PERSONAL DIGITAL CELLULAR PHONES

Yasunori Bito, Naotaka Iwata and Masatoshi Tomita

Kansai Electronics Research Laboratories, NEC Corporation

9-1, Seiran 2-Chome, Otsu, Shiga 520-0833, Japan

ABSTRACT

This paper describes 950 MHz power performance of an enhancement-mode double-doped AlGaAs/InGaAs/AlGaAs heterojunction FET operated at 3.5 V for personal digital cellular phones. The developed 0.5 μm gate length FET exhibited an on-resistance of 1.5 Ωmm and a threshold voltage of +0.09 V. Under single 3.5 V operation, a 19.2 mm gate width FET exhibited an output power of 1.03 W (30.1 dBm) and a power-added efficiency of 64.0 % with an adjacent channel leakage power of -48.7 dBc at 50 kHz off-center frequency.

INTRODUCTION

Personal digital cellular (PDC) phones require small-sized and high efficiency power devices that can be operated at 3.5 V. In addition, a single bias operation is desirable. This eliminates the need for a negative bias voltage supply, thus reducing size and cost of the cellular phone. We reported a single bias operation of a double-doped AlGaAs/InGaAs/ AlGaAs heterojunction FET (HJFET) with a threshold voltage (V_T) of -0.35 V, operated at gate-to-source bias voltage (V_{gs}) of 0.0 V [1]. Furthermore, a positive V_T of an enhancement-mode FET can eliminate the need for a drain bias switch. However, an excellent power performance of an enhancement-mode FET has been hampered due to small drain current as well as high on-resistance (R_{on}) [1]. In this paper, a power-added efficiency (PAE) of 64 % at the PDC criteria is described for a novel enhancement-mode HJFET operated at 3.5 V.

DESIGN and FABRICATION

Figure 1 shows the cross section of the developed HJFET.

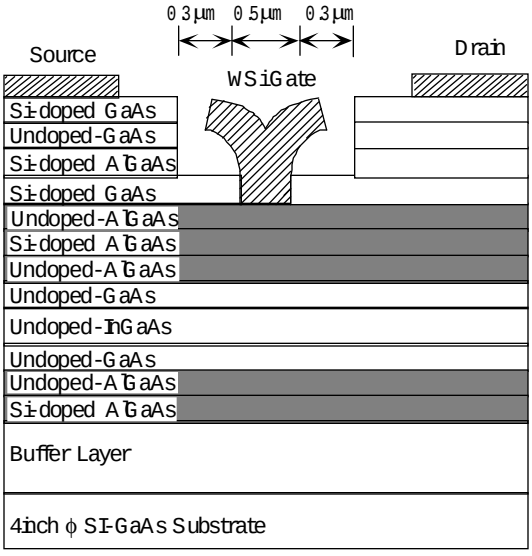

Figure 1: Cross section of the HJFET

For high PAE operation, a reduction of R_{on} is principal [2]. We investigated two novel

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

designs for the double-doped HJFET. The first is a novel multilayer cap consisting of a highly Si-doped GaAs, an undoped GaAs and a highly Si-doped AlGaAs. A double recessed structure was fabricated by electron cyclotron resonance plasma dry-etching with SF_6 and BCl_3 [2]. With these structure, 0.1 Ω·mm reduction of R_{on} was achieved due to a reduction of a contact resistance between the cap and the channel layers. The second is a narrow recessed structure. In this investigation, a total recess width (L_w) was evaluated from 1.0 to 3.4 μm with a gate length (L_g) of 0.5, 0.7 and 0.9 μm, taking account of gate breakdown characteristics. Figure 2 shows a dependence of R_{on} on L_w of HJFETs with and without the multilayer cap. We found that 1.0 μm shrinkage of L_w reduced R_{on} by 0.3 Ω·mm.

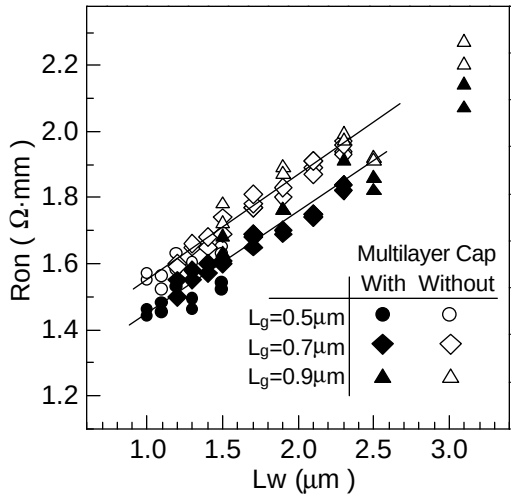

Figure 2: Dependence of R_{on} on L_w of HJFETs with and without multilayer cap

Figure 3 shows a dependence of a gate-to-drain breakdown voltage (BV_{gd}) on gate-to-drain spacing (L_{gdr}) of HJFETs with and without the multilayer cap. There was scarcely any difference between the characteristics with and without the multilayer cap. It was found that the multilayer cap did not degrade BV_{gd}. An HJFET with L_{gdr} of 0.3 μm achieved BV_{gd} of more than 14 V, which was sufficiently high for Li-ion battery operation [3]. The optimized recess structure was determined to be L_w of 1.1 μm with L_g of 0.5 μm and L_{gdr} of 0.3 μm. As a result, the developed HJFET exhibited R_{on} of as low as 1.5 Ω·mm.

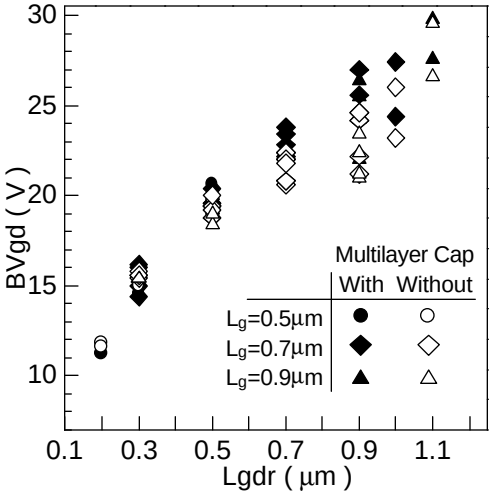

Figure 3: Dependence of BV_{gd} on L_{gdr} of HJFETs with and without multilayer cap

Figure 4 shows transconductance (g_m) and drain current (I_d) as a function of V_{gs}. The device exhibited a positive V_T of +0.09 V with a maximum drain current of 400 mA/mm and a maximum g_m of 500 mS/mm.

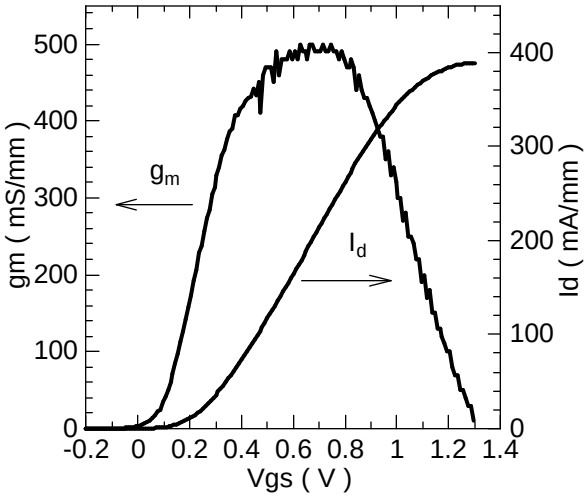

Figure 4: g_m and I_d as a function of V_{gs}

PDC POWER PERFORMANCE

An HJFET with a gate width of 19.2 mm was examined at a source-to-drain voltage (V_{ds}) of 3.5 V with a 950 MHz $\pi/4$-shifted quadrature phase shift keying signal. The device was operated under a quiescent drain current (I_q) of 300 mA (V_{gs} = +0.23 V). Figure 5 shows an output power (P_{out}), PAE, gain and an adjacent channel leakage power at 50 kHz off-center frequency (P_{adj}) as a function of an input power (P_{in}).

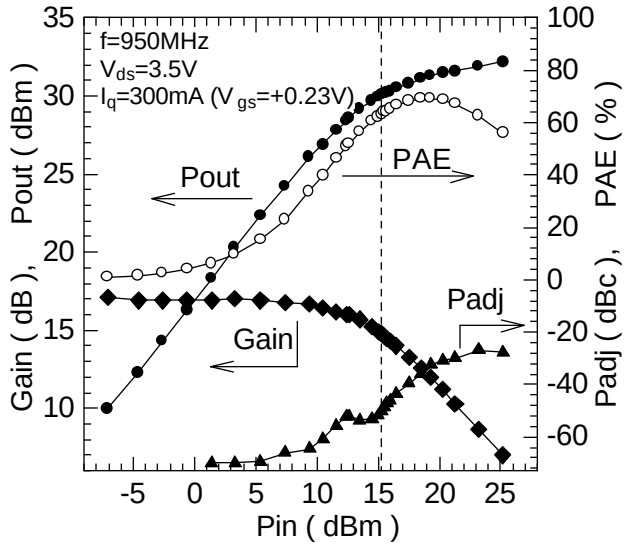

Figure 5: 950 MHz PDC Power Performance

The HJFET exhibited P_{out} of 1.03 W (30.1 dBm), PAE of 64.0 % and an associated gain of 14.6 dB with P_{adj} of -48.7 dBc. The obtained PAE is the best value among power devices for PDC phones, to our knowledge [4]. The device also showed a maximum PAE of 69.2 % with P_{out} of 1.35 W (31.3 dBm).

We reported that the measured PAE at 1 dB gain compression (PAE_{-1dB}) is approximately equal to the calculated maximum drain efficiency (η_d) from class A operation analysis [2]. In class A operation analysis, η_d can be represented as

$$\eta_d = \frac{1}{2} - \frac{I_{DC} \cdot R_{on}}{V_{ds}} \qquad (1)$$

where I_{DC} is the drain DC current under operation. When V_{ds} = 3.5 V, I_{DC} = 0.38 A (this value is I_d at 1 dB gain compression.) and R_{on} = 1.5 Ω·mm were substituted into (1), η_d for the developed HJFET was derived to be 49.2 %, while η_d for the reported HJFET of 47.1% PAE at the PDC criteria was derived to be 41.6 % (*i.e.* V_{ds} = 3.0 V, I_{DC} = 1.6 A, R_{on} = 3.3 Ω·mm) [1]. The PAE at the PDC criteria was reported to be increased by 30 % due to gain compression operation, as compared with PAE_{-1dB}, *i.e.* η_d [2]. Consequently, the high PAE of 64.0 % is ascribed to a low R_{on} of 1.5 Ω·mm.

Furthermore, the V_{ds} dependence of PDC power performance was evaluated from 0.5 to 4.5 V. Figure 6 shows P_{out} and PAE as a function of V_{ds} at PDC criteria. The device exhibited PAE of more than 60 % at V_{ds} of higher than 2.2 V.

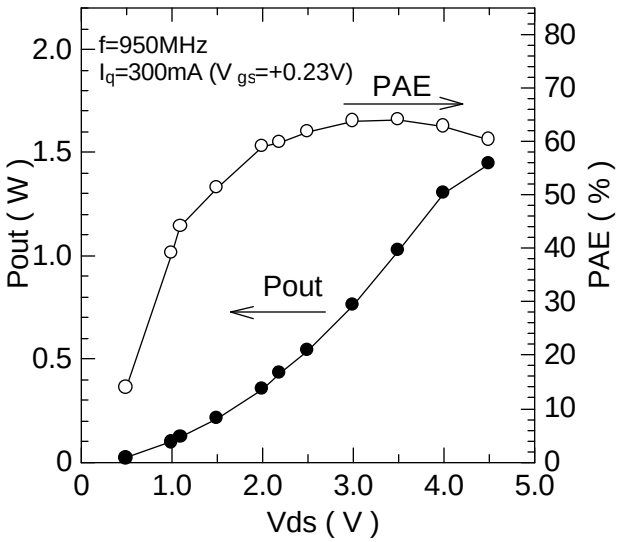

Figure 6: P_{out} and PAE as a function of V_{ds} at the PDC criteria

The I_q dependence of power performance was also evaluated from 50 to 500 mA. Figure 7 shows P_{out} and PAE as a function of I_q at the PDC criteria. The device exhibited relatively flat characteristics for I_q of more than 200mA. Even operated at I_q of 200 mA, a high PAE of

63.7 % with P_{out} of 0.98 W was achieved. These results indicate that the developed enhancement-mode HJFET is promising for personal digital cellular power modules operated at single voltage supply.

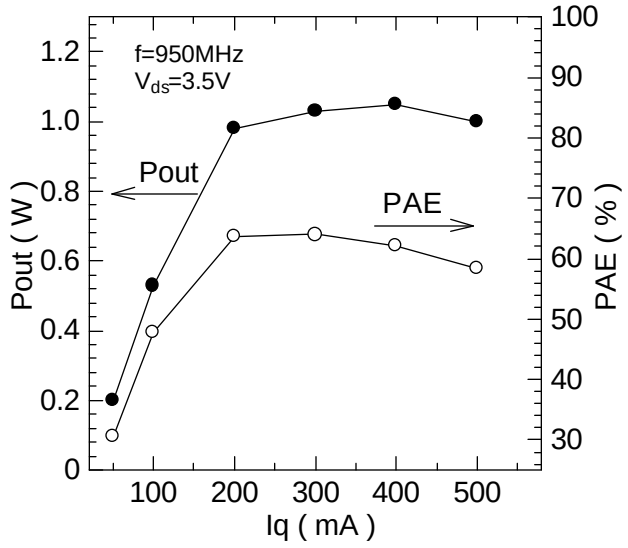

Figure 7: P_{out} and PAE as a function of I_q at the PDC criteria

SUMMARY

We have developed an enhancement-mode power HJFET with R_{on} of 1.5 Ω·mm for PDC phones. Under single 3.5 V operation, the 19.2 mm gate width HJFET exhibited P_{out} of 1.03 W (30.1 dBm) and PAE of 64.0 % with P_{adj} of -48.7 dBc. The device also exhibited PAE of more than 60 % at V_{ds} of higher than 2.2 V.

ACKNOWLEDGMENT

The authors would like to thank Ms. K.Yamaguchi for useful discussions. They are also grateful Drs. T.Uji, M.Ogawa and K.Ueda for their encouragement.

REFERENCES

[1] N.Iwata, K.Inosako and M.Tomita, "Single Low-Voltage Operation Power Hetero-junction FETs for Digital Cellular Applications", 22nd Int. Symp. Compound Semiconductors, pp. 813-816, 1995.

[2] N.Iwata, M.Tomita, K.Yamaguchi, H.Oikawa and M.Kuzuhara, "7 mm Gate Width Power Heterojunction FETs for Li-Ion Battery Operated Personal Digital Cellular Phones", IEEE GaAs IC Symp. Tech. Dig., pp. 119-122, 1996.

[3] K.Mori, M.Nakayama, Y.Itoh, S.Murakami, Y.Nakajima, T.Takagi and Y.Mitsui, "Direct Efficiency and Power Calculation Method and Its Application to Low Voltage High Efficiency Power Amplifier", IEICE Trans. Electron., 1995, vol. E78-C, no. 9, pp. 1229-1236.

[4] N.Iwata, K.Inosako and M.Kuzuhara, "2.2 V Operation Power Heterojunction FET for Personal Digital Cellular Telephones", Electron. Lett., vol. 31, no. 25, 1995, pp. 2213-2214.